URN etd-0407109-183718-1523
Author Li-Hsuan Huang
Author's Email Address No Public.
Statistics This thesis had been viewed 30 times. Download 0 times.
Department
Year 2004
Semester 2
Degree Master
Type of Document Master's Thesis
Language zh-TW.Big5 Chinese
Title A PLL-Based Clock Generator With Voltage Regulator
Date of Defense 0000-00-00
Page Count 104

Keyword
Phase Lock Loops
ripple
phase noise
design
system
charge pump
VCO
Voltage Regulator

Abstract
Every product has different specification, so it is meaningless to design all specification to the best and produce high cost. This paper is to modify some circuit based on product specification in order to make balance of cost and specification.
We start to study how to use the least cost to reduce Locking time and increase locking speed of phase lock loops without modifiying original circuit characteristics. In addition, VCO circuit in the system is a high pass filter. Noise of VCO will make contribution to output frequency. So, we must use technique of designing circuit and modify VCO structure to decrease phase noise and design a phase lock loops with low-jitter characteristic further. Therefore, this study will introduce and discuss each product specification, bandwidth design and stability.
The paper use the function of Voltage Regulator Circuit to improve the characteristic of Phase Lock Loops by adding power on reset circuit and Voltage Regulator circuit. In fact, if Band Width of Low Pass Filter in Phase Lock Loops system is designed small, jitter will decrease while setting speed will increase. In other words, the relationship of locking time and phase noise is trade-off. When power is on, the result of setting speed don’t always achieve our expectation. Therefore, we can try to advance the initial value of predicted oscillator’s frequency in the transient stage of power on. This approach will save the time of which the system compares frequency. For the part of phase detector, it can stable time speedily by adopting synchronism concept to speed up the setting speed in system. By doing so, the initial phase noise can be kept and setting speed in system can be increased.
This is a new idea without relative international papers and I believe this design will make contribution to the design of Phase Lock Loops. Intial ideas will make application in consuming products, such as wake-up system of sleep mode in PDA/micro-control, and apply to make fast stability in changing frequency.
Advisory Committee Yu-Zung Chiou - advisor

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Date of Submission 2005-07-29